Amendments of the Claims:

A detailed listing of all claims in the application is presented below. This listing of claims will replace all prior versions, and listings, of claims in the application. All claims being currently amended are submitted with markings to indicate the changes that have been made relative to immediate prior version of the claims. The changes in any amended claim are being shown by strikethrough (for deleted matter) or underlined (for added matter).

1. (Currently Amended) A semiconductor device deposited on a surface suitable for epitaxial growth having a first lattice constant and a first thermal evaporation rate manufactured by a method comprising the steps of:

a) depositing a lattice-mismatched layer, having a second lattice constant in no-strain state, which is different than ~~of~~ the first lattice constant ~~of the surface~~, wherein the lattice-mismatched layer has a second thermal evaporation rate, wherein the lattice-mismatched layer is deposited until at least one dislocation in the lattice-mismatched layer is created and a desired thickness is reached;

b) depositing a cap layer, having a third lattice constant and a third thermal evaporation rate wherein the third thermal evaporation rate is lower than the second evaporation rate, such that the cap layer nucleates selectively on at least one region of the lattice-mismatched layer such that the at least one dislocation is not covered by the cap layer; and

c) annealing the device at a temperature and duration, such that the at least one dislocation is eliminated by local evaporation of the nearby region of the lattice-mismatched layer.

2. (Original) The semiconductor device of claim 1, wherein the method of manufacture further comprises the step of, prior to step (a), depositing an epilayer on the surface.

3. (Original) The semiconductor device of claim 2, wherein the method of manufacture further comprises the step of, after step (c), overgrowing an additional layer of the epilayer on the device.

4. (Original) The semiconductor device of claim 1, wherein the at least one dislocation is selected from the group consisting of:

a) at least one dislocation network;

b) at least one local dislocation;

c) at least one local defect dipole; and

d) at least one dislocated three-dimensional cluster.

5. (Original) The semiconductor device of claim 1, wherein the difference between the lattice constant of the cap layer in no-strain state and the surface is smaller or of opposite sign than the difference between the lattice constant of the lattice-mismatched layer and the surface.

6. (Original) The semiconductor device of claim 1, wherein step (a) is performed using a growth technique selected from the group consisting of:

a) molecular beam epitaxy deposition; and

b) metal-organic chemical vapor deposition.

7. (Original) The semiconductor device of claim 1, wherein steps (a) and (b) are repeated two times to twenty times.

8. (Original) The semiconductor device of claim 1, wherein steps (b) and (c) are repeated two to forty times.

9. (Original) The semiconductor device of claim 1, wherein steps (a) through (c) are repeated two to forty times.

10. (Original) The semiconductor device of claim 1, wherein the semiconductor device is selected from the group consisting of:

a) a diode laser;

b) a light-emitting diode;

c) a photodetector

d) a light amplifier

e) a far intraband infrared intraband detector;

f) an intraband far infrared emitter;

g) a heterojunction bipolar transistor;

h) a resonant tunneling diode;

k) a solar cell;

l) an optically bistable device;

m) an injection laser; and

n) a vertical cavity surface emitting laser.